What is claimed is:

1. A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the non-volatile memory devices has:

a word gate formed above a semiconductor layer with a gate insulating layer interposed;

an impurity layer formed in the semiconductor layer to form a source region or a drain region; and

control gates in the form of side walls formed along both side surfaces of the word gate;

wherein each of the control gates consists of a first control gate and a second control gate adjacent to each other;

wherein a first insulating layer is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer is disposed between the second control gate and the semiconductor layer;

wherein the thickness of the second insulating layer is less than the thickness of the first insulating layer; and

wherein an uppermost layer of the second insulating layer is a charge transfer protection film.

2. The semiconductor device as defined in claim 1,

wherein the first insulating layer is a stack of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film.

3. The semiconductor device as defined in claim 2,

wherein the second insulating layer is a stack of a silicon oxide film, a silicon nitride film and the charge transfer protection film, the thickness of the charge transfer protection film being less than the thickness of the second silicon oxide film of the first insulating layer.

4. The semiconductor device as defined in claim 1,

wherein the charge transfer protection film is further provide on a surface of the first control gate.

5. The semiconductor device as defined in claim 1,

wherein the charge transfer protection film is one of a silicon oxide film and a silicon oxide nitride film.

6. The semiconductor device as defined in claim 2,

wherein the charge transfer protection film is further provide on a surface of the first control gate.

7. The semiconductor device as defined in claim 3,

wherein the charge transfer protection film is further provide on a surface of the first control gate.

8. A method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising:

(a) forming a gate insulating layer above a semiconductor layer;

(b) forming a first conductive layer above the gate insulating layer;

(c) forming a stopper layer above the first conductive layer;

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of that stopper layer and that first conductive layer;

(e) forming a first insulating layer by stacking a first silicon oxide film, a silicon nitride film, and a second silicon oxide film over the entire surface of the memory region;

(f) forming a second conductive layer above the first insulating layer, and then anisotropically etching the second conductive layer into side-wall-shaped first control gates on both side surfaces of the first conductive layer and on the semiconductor layer with the first insulating layer interposed;

(g) using the first control gate as a mask to remove a surface portion of the second silicon oxide film of the first insulating layer, and defining part of the remaining first insulating layer as a second insulating layer;

(h) forming a third conductive layer over the entire surface of the memory region, and then anisotropically etching the third conductive layer into a second control gate on a side surface of each of the first control gates and on the semiconductor layer with the second insulating layer interposed;

(i) forming an impurity layer in the semiconductor layer to form a source region or a drain region;

(j) forming a third insulating layer over the entire surface of the memory region and then removing part of the third insulating layer to expose part of the stopper layer; and

(k) removing the stopper layer, forming a fourth conductive layer over the entire surface of the semiconductor layer, and then patterning the fourth conductive layer to form a word line.

9. A method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising:

(a) forming a gate insulating layer above a semiconductor layer;

(b) forming a first conductive layer above the gate insulating layer;

(c) forming a stopper layer above the first conductive layer;

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of that stopper layer and that first conductive layer;

(e) forming a first insulating layer by stacking a first silicon oxide film, a silicon nitride film, and a second silicon oxide film over the entire surface of the memory region;

(f) forming a second conductive layer above the first insulating layer, and then anisotropically etching the second conductive layer into side-wall-shaped first control gates on both side surfaces of the first conductive layer and on the semiconductor layer with the first insulating layer interposed;

(g) using the first control gate as a mask to remove part of the second silicon oxide film of the first insulating layer and expose part of the silicon nitride film of the first insulating layer, forming a charge transfer protection film on the exposed portion of the silicon nitride film of the first insulating layer, and then defining part of the remaining first insulating layer and the charge transfer protection film as a second insulating layer;

(h) forming a third conductive layer over the entire surface of the memory region, and then anisotropically etching the third conductive layer into a second control gate on a side surface of each of the first control gates and on the semiconductor layer with the second insulating layer interposed;

(i) forming an impurity layer in the semiconductor layer to form a source region or a drain region;

(j) forming a third insulating layer over the entire surface of the memory region and then removing part of the third insulating layer to expose part of the stopper layer; and

(k) removing the stopper layer, forming a fourth conductive layer over the entire surface of the semiconductor layer, and then patterning the fourth conductive layer to form a word line.

10. The method of manufacturing a semiconductor device as defined in claim 9, wherein the charge transfer protection film is one of a silicon oxide film and a silicon oxide nitride film.

11. The method of manufacturing a semiconductor device as defined in claim 10, wherein the charge transfer protection film is formed by a chemical vapor deposition method.

12. The method of manufacturing a semiconductor device as defined in claim 10, wherein the charge transfer protection film is formed by a thermal oxidation method.